

**INTERNATIONAL
STANDARD**

**ISO/IEC
13213**

**ANSI/IEEE
Std 1212**

First edition
1994-10-05

**Information technology –
Microprocessor systems – Control
and Status Registers (CSR) Architecture
for microcomputer buses**

*Technologies de l'information –
Systèmes à microprocesseurs – Architecture
des registres de commande et d'état
pour bus de micro-ordinateur*



Reference number
ISO/IEC 13213: 1994(E)
ANSI/IEEE
Std 1212, 1994 Edition

Abstract: The document structure and notation are described, and the objectives and scope of the CSR Architecture are outlined. Transition set requirements, node addressing, node architectures, unit architectures, and CSR definitions are set forth. The ROM specification and bus standard requirements are covered.

Keywords: CSR Architecture, bus architecture, bus standard, interoperability, microprocessors, node addressing, registers, transaction sets

The Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street, New York, NY 10017-2394, USA

Copyright © 1994 by the Institute of Electrical and Electronics Engineers, Inc.
All rights reserved. Published 1994. Printed in the United States of America

ISBN 1-55937-448-9

No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of the publisher.

October 5, 1994

SH94220